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epitaxial layer to form a Schottky diode, comprising diverting current from the body-to-drain pn junction of the DMOS transistor with the Schottky diode that is co-integrated with the DMOS transistor when the source becomes more positive than a drain of the DMOS transistor [and the gate has not induced a channel region between the source region and the drain region]

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Fig. 18
21. (New) A method of operating a [vertical DMOS transistor] in an integrated circuit, the DMOS transistor having an epitaxial layer of a first conductivity type formed over a substrate, a deep barrier region formed within adjoining surface portions of the substrate and the epitaxial layer, a deep drain region extending from a surface of the epitaxial layer to outer peripheral regions of the deep barrier region to define a well region within the epitaxial layer, a body region of a second conductivity type formed within the well region, first and second source regions of the first conductivity type positioned at a surface of the well region and within the body region, first and second portions of gate electrodes positioned above the first and second source regions, respectively, the body region, and the well region, a conductive drain contact coupled to the deep drain region, and a metallic source contact coupled to the first and second source regions and to a central portion of the well region, the metallic source contact forming a Schottky diode, and the body region forming a pn junction diode with the deep drain region, the method comprising:

diverting current from the body-to-drain pn junction of the vertical DMOS transistor with the Schottky diode that is co-integrated with the DMOS transistor when the source ^{regions} [region] becomes more positive than the deep drain region of the vertical DMOS transistor.

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22. (New) A method of operating a [vertical DMOS device] in an integrated circuit for reducing the effects of parasitic devices in the integrated circuit that drive an inductive load, the device including an epitaxial layer formed on a substrate; a well region formed by a deep drain region extending from a surface of the epitaxial layer and over a peripheral area of a deep barrier region located ^{between} [within] the epitaxial layer and the substrate; a body region within the well region, the body region containing first and second source regions; [a plurality of insulated gate electrodes formed over outer portions and inner central portions of the first and second source regions, respectively], the body region, and the well region, a guard ring in a central

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surface portion of the well region and surrounded by the body region; a first metallic contact coupled to the deep drain region; and a Schottky metallic contact coupled to the source regions and to the central surface portion of the well region between the insulated gate electrodes and contacting the guard ring, the Schottky metallic contact forming a Schottky diode, and the body region forming a pn junction diode with the deep drain region, the method comprising:

diverting current from the body-to-drain pn junction of the vertical DMOS transistor with the Schottky diode that is co-integrated with the vertical DMOS transistor when the first and second source regions become more positive than the deep drain region of the vertical DMOS transistor.

23. (New) A method of operating a [vertical DMOS device] in an integrated circuit for reducing operational effects of parasitic devices associated with the integrated circuit, the device including a well region defined by a buried isolation region having an overlapping deep drain region within an epitaxial layer; a body region containing first and second source regions within the well region; insulated gates formed over a portion of the first and second source regions; and a Schottky contact coupled to a central portion of the well region and spaced from the body region, the Schottky contact defining a portion of a Schottky diode within the epitaxial layer having operational characteristic means for reducing operational characteristics of parasitic devices associated with the [IC] circuits, and the body region forming a pn junction diode with the deep drain region, the method comprising:

diverting current from the body-to-drain pn junction of the vertical DMOS transistor with the Schottky diode that is co-integrated with the vertical DMOS transistor when the first and second source regions become more positive than the deep drain region of the vertical DMOS transistor.

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24. (New) A method of operating a [vertical DMOS transistor] in an integrated circuit, the vertical DMOS transistor including an epitaxial layer of a first conductivity type formed over a substrate of a second conductivity type; a drain region of ^{the} a first conductivity type formed within the epitaxial layer; a body region of the second conductivity type formed within the epitaxial layer and forming a pn junction diode with the drain region; a source region of the

first conductivity type formed within the body region; a gate electrode positioned above the source region, the body region, and the epitaxial layer; a conductive drain contact coupled to the drain region; and a metallic source contact coupled to the source region and to the epitaxial layer, the metallic source contact having contact with the epitaxial layer at a surface of contact, the surface of contact forming a rectifying barrier in the form of a Schottky diode, the method of operating comprising:

conducting current through the Schottky diode when a forward bias is applied from the metallic source contact to the conductive drain contact.

25. (New) A method of operating a [vertical DMOS transistor] in an integrated circuit, the DMOS transistor including an epitaxial layer of a first conductivity type formed over a substrate of a second conductivity type; a drain region of ^{the} [a] first conductivity type formed within the epitaxial layer;

a body region of the second conductivity type formed within the epitaxial layer and forming a pn junction diode with the drain region, the body region having an annular body region surrounding a central portion of the epitaxial layer; a source region of the first conductivity type formed within the body region, the source region including two annular source regions separated by an annular region of the second conductivity type; a gate electrode positioned above the source region, the body region, and the epitaxial layer, the gate electrode having two annular gate electrodes positioned, respectively, above the two annular source regions; a conductive drain contact coupled to the drain region; and a metallic source contact coupled to the source region and to the epitaxial layer, the metallic source contact having contact with the epitaxial layer at a surface of contact at a central portion of the epitaxial layer to form a rectifying barrier in the form of a Schottky diode, the method comprising:

conducting current through the Schottky diode when a forward bias is applied from the metallic source contact to the conductive drain contact to divert current from the body-to-drain pn junction of the DMOS transistor with the Schottky diode that is co-integrated with the DMOS transistor as the source region becomes more positive than the drain region of the vertical DMOS transistor.